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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,203	01/28/2004	Yutaka Arima	402952/SAKAI	7648

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EXAMINER	
WILSON, SCOTT R	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 09/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/765,203	ARIMA, YUTAKA	
	Examiner	Art Unit	
	Scott R. Wilson	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-9 and 12* is/are rejected.

7)☒ Claim(s) *3,10 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/28/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2 and 4-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Fukase. As to claim 1, Fukase, Figure 3B and col. 2, lines 21-33, discloses a metal oxide semiconductor transistor comprising a semiconductor substrate (101), a source area (102) formed in a device area of the semiconductor substrate, a drain area (103) formed in the device area; a gate layer (106) formed on and across the device area between the source area and the drain area; a control gate layer (111) having a first part including a first end of the control gate layer, shown over the notation "L1" and hereinafter referred to as the L1 portion of the control gate, and a second part including a second end of the control gate layer, shown over the notation "L2" and hereinafter referred to as the L2 portion of the control gate, the first part (L1) being formed on the device area between the gate layer and at least one of the source area and the drain area, the first end being disposed so that there is a gap, embodied as the distance from the left-hand edge of the L1 portion of the control gate to the left-hand edge of the left-hand source area (102), between the first end and an edge of the device area; and a diffusion area formed in the device area between the gate area and the control gate area, embodied as the drain (103) between the gate area (106) under the L1 portion of the control gate and the L2 portion of the control gate, which is part of the control gate.

As to claim 2, Fukase, Figure 3B, discloses that the gate layer (106) and the control gate layer (111) are formed on a common plane, namely the upper surface of the substrate (101).

As to claim 4, Fukase, Figure 3B, discloses that the second part (L2) is formed on the device area between the drain area (103) and the gate layer (right-hand gate (106), and the second end is disposed

so that there is a gap between the second end and an edge of the device area, embodied as the distance from the right-hand edge of the L2 portion of the control gate to the right-hand edge of the right-hand source area (102).

As to claim 5, the device of Fukase, Figure 3B, would necessarily have wiring connecting the gate layer (106) and gate control layer (111) to external electrodes which would enable voltages to be applied and allow the device to operate. This wiring would necessarily be formed outside the device area.

As to claim 6, Fukase, Figure 7, discloses an embodiment in which the control gate electrodes (9), which correspond to the control gate electrodes (111) of prior art Figure 3B, are formed as wordlines (col. 6, lines 38-39) which have portion formed outside the device area, and have portions which are formed on opposite sides of the device area.

As to claim 7, Fukase, (Abstract), discloses a split gate type transistor, for which it is recognized in the art that the split control gates may be shorted together in certain implementations. The implementation in which the two control gates are shorted together is within the scope of the control gate layer having a third part connecting the first part and the second part outside the device area.

As to claim 8, Fukase, col. 1, lines 31-32, discloses that the source and drain are both of the same conductivity type. Fukase, Figure 3B, discloses that the impurity diffusion of the source area is larger than the impurity diffusion of the drain area, which is within the scope of the drain area having lower impurity concentration than the source area.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukase in view of Kachelmeier. As to claim 9, Fukase, Figure 3B and col. 2, lines 21-33, discloses a metal oxide semiconductor transistor comprising a semiconductor substrate (101), a source area (102) formed in a device area of the semiconductor substrate, a drain area (103) formed in the device area; a gate layer (106) formed on and across the device area between the source area and the drain area. Fukase does not disclose expressly a control channel area formed in the device area between the gate layer and at least one of the source area and drain area, where the control channel area has a threshold value that gradually changes in a longitudinal direction of the gate layer. Kachelmeier, Figure 2, discloses a MOS transistor with a variable thickness gate oxide layer, which would necessarily have a threshold that longitudinally varied. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the device of Fukase with the variable threshold structure of Kachelmeier. The motivation for doing so would have been to reduce the entry into the gate oxide layer of hot electrons (Kachelmeier, paragraph 0004). Therefore, it would have been obvious to combine Kachelmeier with Fukase to obtain the invention as specified in claim 9.

As to claim 12, the gate oxide insulating layer of Kachelmeier, Figure 2, has a thickness that gradually changes in the longitudinal direction.

Allowable Subject Matter

Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed invention with the second of two parts of the control gate layer disposed outside the device area.

Claim 10 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed invention with two channel areas, one with gradually increasing threshold and the other with gradually decreasing threshold.

Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed invention in which the control channel area includes a channel diffusion area that has an impurity concentration which varies longitudinally.

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 571-272-1925. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

srw
September 10, 2004